

An Additional 12% Power Reduction in Practical Digital Chips with a Low-Power Design Using Post-Fabrication Clock-Timing Adjustment

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In order to solve the clock-skew problem, which becomes more and more serious for sub-100 nm processes, we have proposed a post-fabrication clock-timing adjustment technique and have been improving it to expand its applications. Several kinds of test chips have been designed and fabricated, and the promising experimental results obtained for these chips have already been presented in several papers. In this paper, the adjustment technique is applied to practical circuits with a low-power design. Conducted experiments demonstrate an additional reduction in power consumption of 12% even for chips with a low-power design, and the effectiveness of the proposed method is confirmed with actual chips.

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1. Introduction

Recently, the problem of clock skew, referring to fluctuations in clock timing, is becoming ever more serious with the increased speeds and complexity of digital LSIs. As a result, operation yields (the ratio of chips that can operate according to design specifications) for digital LSIs are decreasing, leading to rises in chip prices. One major cause of clock skew are manufacture variations, which alter delay timings, the driving ability, wiring resistances and the parasitic capacitances of each transistor. In order to solve the clock-skew problem for digital LSIs, the Millennium Research for Advanced Information (MIRAI) project has proposed a post-fabrication clock-timing adjustment using genetic algorithms (GA).^{1,2)} The method involves adjusting programmable delay circuits inserted in the clock line of a chip which makes it possible to fine-tune clock input timing with the genetic algorithm³⁾ after the chip is fabricated. However, the increases in adjustment times that are incurred when more programmable delay circuits are incorporated within large-scale LSIs are a serious issue.

To overcome this problem, we have proposed a speed enhancement technique for the post-fabrication clock-timing adjustment that reduces the number of adjustment points and improves the GA.⁴⁾ Adjustment experiments using a developed simulator demonstrate that our method can improve search performance greatly. In this paper, the adjustment technique is applied to practical circuits with a low-power design. The purpose of the study is to report on the achievement of an additional reduction in power consumption for the practical chips, and the effectiveness of the speed enhancement technique with actual chips.

Section 2 explains the technique of post-fabrication clock-timing adjustment for digital LSIs, and the speed enhancement technique for large-scale LSIs. Section 3 describes a practical circuit with a low-power design. Section 4 reports on the results of adjustment experiments with actual chips, while §5 provides a summary.

2. Post-Fabrication Clock-Timing Adjustment

The post-fabrication clock-timing adjustment technique may be considered as an expanded trimming technique, and can automatically and simultaneously determine the values for multiple trimming devices. In this method, a chip is designed and fabricated with programmable delay circuits inserted into all the flipflops, in order to fine-tune the timing of clock signals. After the chip is fabricated, the inserted programmable delay circuits are optimally adjusted by executing a GA, which is a robust search algorithm within artificial intelligence. Clock timing is not measured directly, but the results of function tests are utilized to adjust clock timing. For instance, unit delays of 30 ps or less have been reported in the literature,²⁾ while there are various methods of implementing programmable delay circuits. Similarly, there are a number of methods for setting the delay value for the programmable delay circuit, such as one reported in ref. 1.

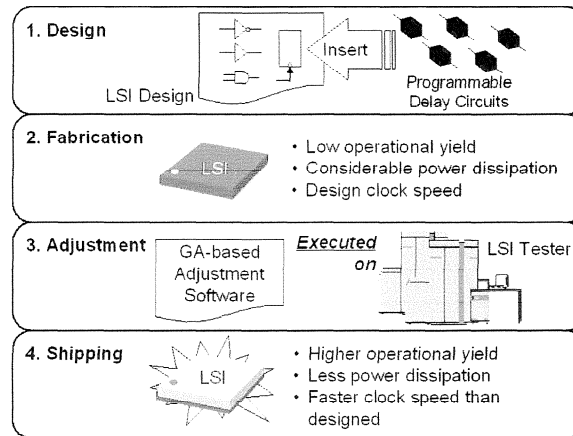


Fig. 1. Post-fabrication clock-timing adjustment for digital LSIs.

2.1 Procedure for the clock-timing adjustment

Figure 1 depicts an overview of post-fabrication clock-timing adjustment. First, programmable delay circuits (delayers) are inserted into a standard LSI designed by normal methods. The values of the programmable delay circuits are not determined at that time. Next, LSI chips are fabricated according to standard procedures. When the chips are tested after fabrication, the values of the programmable delay circuits are determined by the GA-based adjustment software, which is executed on the LSI tester. These values do not change during normal chip operation. Finally, the chips are shipped after adjustment, ensuring not only increased operational yields but chips that can operate at lower power-supply voltages.

Figure 2 outlines the adjustment for a pipeline-type circuit. The clock signal would arrive earlier than the data signal from the combinatorial circuit at the previous flipflop if there is a delay due to a manufacture variation in the combinatorial circuit between the flipflops. Thus, the indefinite value will differ from the value that is initially input to the flipflop, and this would cause the whole circuit to malfunction. However, it is possible to fine-tune the programmable delay circuit inserted within the clock line in order to delay the input timing of the clock signal to the flipflop that has the indefinite value. The delay circuit absorbs the delay due to the adjacent combinatorial circuit, and so prevents the whole circuit from malfunctioning. This adjustment method is also effective when delays due to variations in the clock tree cause circuit malfunctions.

However, there are numerous locations where programmable delay circuits are necessary within a chip, and the optimal values for each delay circuit are closely interrelated. Thus, in order to obtain the optimal value for each delay, it is necessary to solve a search problem within a vast search space. However, by using a genetic algorithm for the adjustment software, it is possible to quickly find the optimal delays for multiple programmable delay circuits. The advantage of using a genetic algorithm for the post-fabrication clock-timing adjustment of

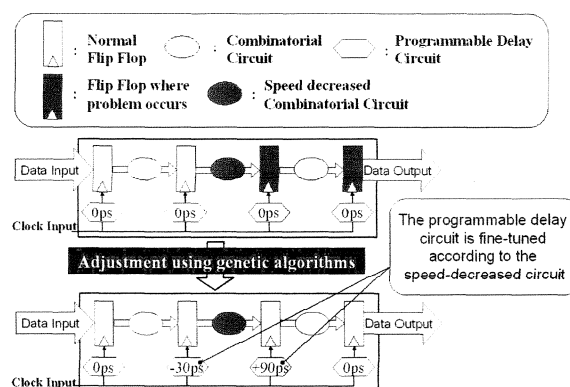


Fig. 2. Adjustment using GA.

digital LSIs is that the necessary adjustment operations can be carried out based on output data signals which can easily be measured with fabricated LSIs.

2.2 A speed enhancement technique for large-scale circuits

There is a problem, however, in that adjustment times increase markedly for large-scale circuits, as the number of adjustment points increase. In order to overcome this problem, we have proposed a speed enhancement technique for the post-fabrication clock-timing adjustment so that it can also be applied to large-scale circuits.⁴⁾ There are three features to the proposed technique: (1) When designing LSIs, it is possible to limit the number of adjustable delay circuits by utilizing static timing analysis (STA) results. Accordingly, adjustment times can be shortened, while the area required for the delay circuits can be reduced. (2) We have developed a simulator that is capable of quickly simulating adjustments without logic simulations. The simulator makes it easy to confirm the effects of feature (1) at the design stages, and the optimum number of delay circuits can be determined. (3) We have improved the distribution in the initial population for the GA when adjusting delay circuits. The convergence speed of the GA is enhanced by this, making it possible to shorten the post-fabrication adjustment time. Adjustment experiments using the developed simulator demonstrate that our method can improve search performance greatly.

The purpose of the present paper is to report on the achievement of an additional reduction in the power consumption of practical chips, and on the effectiveness of the speed enhancement technique with actual chips. As explained in the next section, these practical chips were fabricated for this study.

3. DCT Test Chip Design

The application target is a discrete cosine transform (DCT) circuit with a low-power design.⁵⁾ Table I summarizes the specifications of the chip, and Fig. 3 is a photomicrograph of the chip. The photo shows that the chip contains eight DCT blocks arranged side by side.

Table I. Design Specifications for the DCT test chip.

Clock frequency (MHz)	200 (worst case): design constration
Process	90 nm 6-layer CMOS technology
Die size (mm^2)	5×5
Gate count (Mgates)	2.41
Power-supply (V)	1.0 (core blocks); 2.5 (I/O blocks)

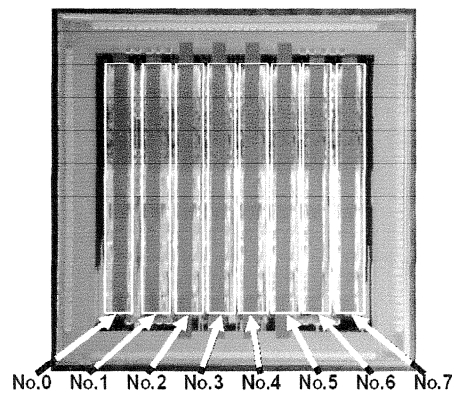


Fig. 3. Photomicrograph and eight blocks of the DCT test chip.

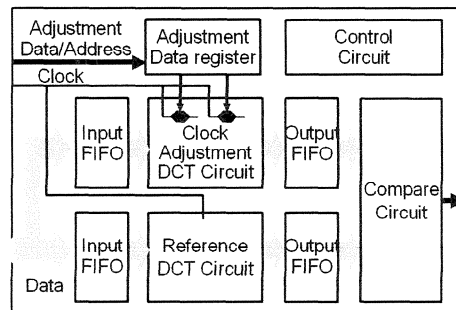


Fig. 4. Block diagram of the DCT test chip.

This chip is a revised version, and the first implementation has already been reported.⁶⁾

Figure 4 shows a block diagram of the DCT circuit. The circuit block contains a “timing-adjustable” DCT and a reference DCT, which accelerate iterative function tests to compare the outputs from the two DCT circuits and to count errors with hardware counters. One DCT has programmable delay circuits while the other does not. The comparators were built-in to compare the output results from the two DCTs. The design target for clock frequency was 200 MHz.

The DCT contains 1,031 programmable delay circuits. A programmable delay circuit is

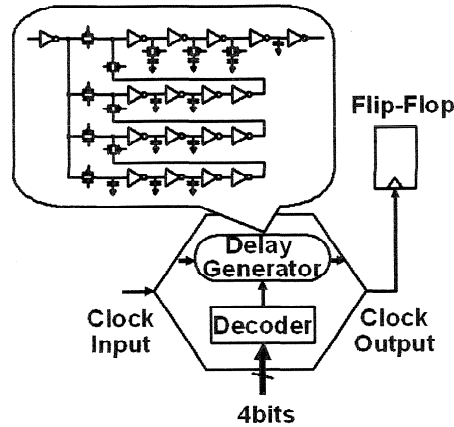


Fig. 5. Programmable delay circuit.

shown in Fig. 5. As a large number of delay circuits are required, a simple 4-bit digital control circuit and a delay generator were employed as an adjustment circuit. The adjustment timing step was designed to execute adjustments ranging from 320 to 1,015 ps. The area for the programmable delay circuit is about 7 times larger than that for the flipflops. The overhead for inserting 1,031 programmable delay circuits is 17% of the total chip area. However, we have restricted the adjusting delayers to just 300 with the speed enhancement technique as has been noted in §2.2. Therefore, the area overhead for the 300 delayers is just 5% of the total chip area.

4. Experimental Results

4.1 Experimental conditions

Figure 6 is a block diagram of the experimental system. The experimental system consists of a printed circuit board (PCB) on which the chip is mounted, a PCB to control the test chip, a power supply for the two PCBs, a pulse generator to generate the clock signal, and a computer to control these instruments and to execute the GA-based adjustment software. 10 test chips were measured, and the results from 58 DCTs were statistically processed. The adjustment will be finish if the adjusting chip passes the function test or the iterations of function test reaches to limitation of 5000 times.

4.2 Clock-timing adjustment for practical chips

Figure 7 presents the experimental results in terms of operational yield dependency on the power-supply voltage. The maximum yield improvement is 50% at 0.98V, and the maximum power-supply voltage reduction is 0.06 V. The maximum reduction in power consumption will be 12% if the power consumption of an LSI varies in proportion to the square of the power-supply voltage.⁷⁾ To verify this result of power reduction, we have conducted an experiment measuring the power consumption. Figure 8 shows a distribution of power reduction for suc-

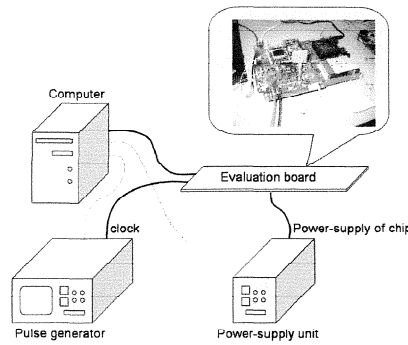


Fig. 6. Block diagram of the experimental system.

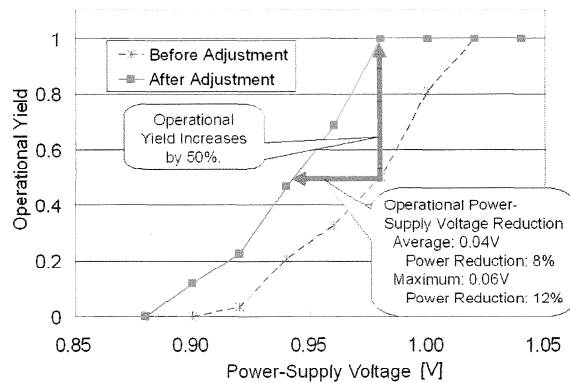


Fig. 7. Operational yield dependency on power-supply voltage using the adjustment.

cessfully adjusted chips. As can be seen, the maximum reduction in power consumption was certainly about 12%.

The chip has eight DCT circuits, and Figs. 9(a) and 9(b) demonstrates the differences among these. The eight lines form four groups of two. Before adjustment, there is a difference of 0.08 V between the two outermost circuits and the two innermost circuits due to IR drop. After adjustment, the difference reduces to 0.07 V.

The elapsed adjustment time was 5 min, but, based on previous experiments,²⁾ we predict the adjustment time on an LSI tester to be just 0.5 s. This indicates that a commercial LSI tester that simultaneously tests 32 chips can adjust the chips at a rate of 15 ms per chip.

4.3 Comparison of the operational yield with the speed enhancement technique and the conventional technique

Table II presents the operational yield increases for adjustment at 0.96 V with the speed enhancement technique and with the conventional technique. The speed enhancement technique reduces the number of delayers from 1,031 to 300, and improves the GA. As this table

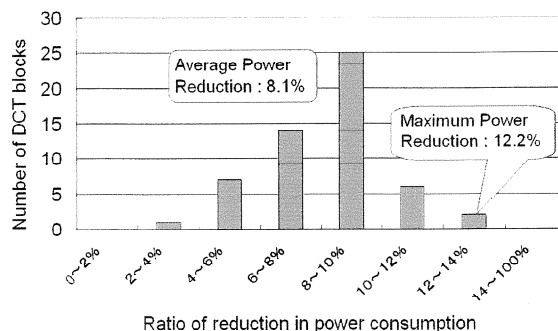


Fig. 8. Measured distribution of power reduction after adjustment.

Table II. Comparison of the operational yield after adjustment at power-supply voltage of 0.96 V.

	Conventional technique	Speed enhancement technique
The operational yield (%)	33	69

shows, the operational yield after adjustment using the conventional technique is 33%. There was no chip that was able to be successfully adjusted with the conventional technique with limitation of 5000 iterations for function tests. In contrast, the operational yield after adjustment based on the speed enhancement technique is 69%. Thus, by applying the speed enhancement technique, the yield improved by 36%.

Figure 10 is a number distribution that shows the iterations of function tests executed during adjustment. Clearly, the number of function tests for the speed enhancement technique is less than the number required for the conventional method. These results demonstrate the effectiveness of the speed enhancement technique with actual chips.

5. Conclusions

In applying the post-fabrication clock-timing adjustment to the test circuits with 1,031 programmable delayers based on a commercial low-power logic design, an additional 12% power reduction was achieved. In addition, the effectiveness of the adjustment speed enhancement technique was confirmed with actual chips. Accordingly, the present results demonstrate that the adjustment method is practically useful for practical chips.

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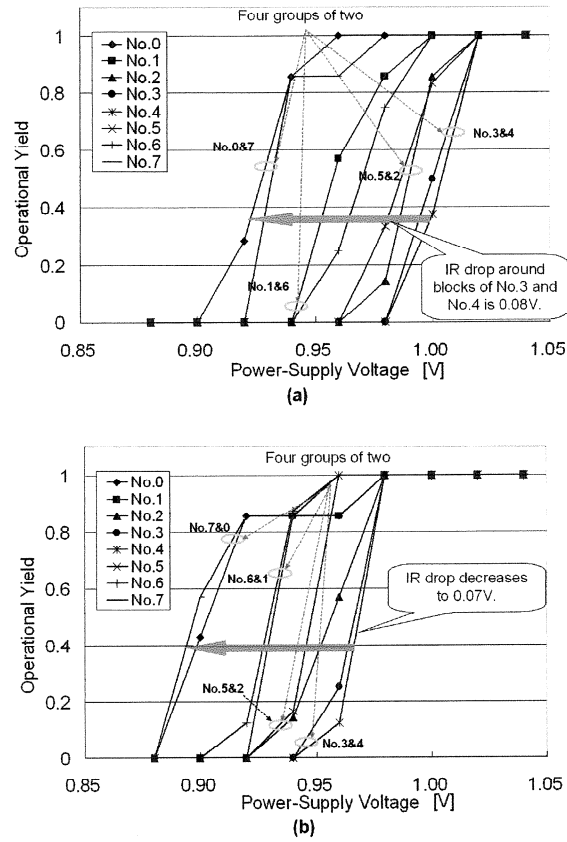


Fig. 9. Adjustment effect dependency on block position: (a) before adjustment and (b) after adjustment.

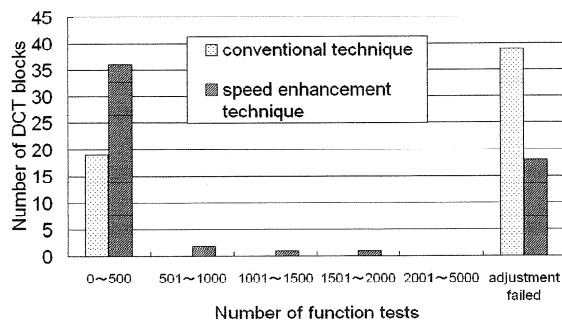


Fig. 10. Number distribution of function test iterations for adjustment at power-supply voltage of 0.96 V.

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